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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,462	04/08/2004	Guido D'Albore	03MAR43253801	7256

27975 7590 08/22/2007

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
08/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,462	D'ALBORE ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,15-22 and 25-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,15-22 and 25-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/7/2007 has been entered.

Claims 1-12, 15-22, and 25-31, are currently pending.

Response to Arguments

Applicant's arguments filed 5/7/2007 have been fully considered but they are not persuasive.

The prior art reference of Wong teaches amended claims 1,15, and 25,as the amendment claims have merely been modified by the limitations of previous claims 13,14,23,24, 32, and 33. Applicant argues that Wong does not teach the amended claims as the limitation of "the flag represents binary information associated to a subroutine that used a patching mechanism having a respective flag associated therewith" (page 11, ¶1 of response). Applicant stated that Wong, in contrast, compares an address provided by a processor with each break-out address to determine a breakout condition (page 10, underlined portion of Wong). Applicant goes on to state advantages of the invention and the difference of Wong and the present invention as claimed. Nonetheless, the Examiner maintains that the Wong reference teaches the amended flag

limitation as the -flag-- limitation may be broadly interpreted as a matching address required to breakout of the subroutine that is patched by the system of Wong. An address is essentially an arrangement of binary information (thus the flag, as interpreted by the Examiner, represents binary information) associated to a subroutine (the break-out address is associated with a subroutine since a portion of the subroutine that is replaced uses the break-out address to execute updated/repaired code instead of the previous code as discussed by Wong. The subroutine uses a patching mechanism which is defined by ROM instructions (patch code are stored as ROM instructions as shown in Wong, figure 6).

Further, each patching mechanism (e.g. set of patch instructions) has a respective flag (e.g. respective break-out address) associated therewith as shown in figure 8 (each set of patch code has a corresponding break-out address to which the patch code will be executed when the address to be executed matches the break-out address - see ¶45 of Wong.

Thus, it is apparent that Applicant has not limited the claims to clearly distinguish the present invention from the prior art teachings of Wong. Specifically, Applicant lists numerous elements of the present invention that distinguishes the invention over that of Wong. Specifically, Applicants mention that Wong maps to a portion of patch code to ROM space whereby the present invention does not require to perform the mapping (stated by the Applicant on page 11, ¶3, of the present response). However, such a limitation is not present in the invention as currently claimed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12, 15-22, and 25-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Wong et al. (U.S. Patent Application Publication No. 2004/0210720).

As per claims 1 and 16, Wong teaches **ROM instructions stored in a non-volatile memory** BROM 602 and/or PROM 608 **that stores instruction groups defining patching functionalities** (patch load instructions 622 and 624, respectively, of figure 6), **an extended memory portion** 406 (figure 4) **storing extended instructions** (i.e. patch code - ¶30), **and an additional memory portion** 418. Wong teaches **checking a flag** (checking executing addresses with the break-out addresses [e.g. "flags"] to determine when patch code is to be run - ¶31) **stored in the additional memory portion** 418 (¶31), **where the flag indicates a need for executing the extended instructions in the extended memory portion** 406, which contains extended instructions 420 - ¶31. Further, Wong teaches **altering processing of the ROM instructions** (BROM and PROM) **in the first non-volatile memory portion and the extended memory portion based on the flag** - ¶31-32. Once the execution of the BROM or PROM memory gets to a break-out address as indicated by the flag of the additional memory 418 (figure 9), processing switches to the patching instructions of the extended memory portion 406 for execution (figure 10).

Additionally, Wong teaches:

the flag represents binary information (i.e. an address is a binary series) **associated to a subroutine** (patch code - step 1002) **that uses a patching mechanism** (element 410 uses patch routine as depicted in figure 9 and figure 10) **defined by the ROM instructions** (since loading of patch code instructions are stored in ROM instructions - figure 6); and

each patching mechanism (set of patch instructions) **has a respective flag** (break-out address) **associated therewith**. Referring to figure 8, each set of patch code has a corresponding flag - (BRK_OUT_ADDR_N[15:0]) - ¶45.

As per claim 2, the **electronic device** 302 (figure 4) **comprises a processor** 402 (¶29).

As per claim 3, **the first memory portion** (BROM and PROM) **comprises a read only memory** - ¶40.

As per claim 4, **the instruction groups comprise subroutines** as the instruction groups result in the execution of the subroutine shown in figure 7 to load the patching information before execution. Refer also to ¶¶42-44.

As per claims 5,6,17, and 26, **the additional memory portion** 418 **comprises** volatile memory as it may be stored inside RAM 406 - ¶30.

As per claims 7,18, and 27, the **additional memory portion** 418 may alternatively **comprise a non-volatile memory** - ¶30.

As per claim 8, the **additional memory portion may be EEPROM** or **flash memory** (end of ¶25).

As per claims 9,19, and 28, **the flag** (break-out address) **indicates whether the instructions in the first nonvolatile memory portion** (BROM or PROM) **or the instructions**

in the extended memory portion are to be executed. If the present address is not indicated by the flag (i.e. present address does not equal a break-out address), the BROM/PROM continues execution, but when the present addresses equals a break-out address, the execution of a patch instruction(s) occurs - ¶31.

As per claims 10,20, and 29, **ROM instructions in the first non-volatile memory portion define a calling ROM based subroutine** (i.e. a function call - ¶32, further it is well known in the art that ROMs comprise subroutines/functions) **and wherein the extended instructions in the extended memory portions reuses the calling ROM based subroutine without resulting in recursive actions** (patch ROM code may reuse any original program code - stored on the original BROM/PROM - ¶32). Recursive actions are avoided since after the patch code is executed, control is returned to the very next address before the break-out - ¶32.

As per claims 11,21, and 30, **the ROM instructions in the first non-volatile memory portion define a calling ROM based subroutine** (as discussed directly above); **and wherein the calling ROM subroutine is executed during execution of the extended instructions in the extended memory portion** (¶32). Wong teaches that the patch code (extended instructions) can call any function or perform any operation (from the original code) as the extended instructions are an extension of the address space of the ROM 404 - figure 4 and ¶32. During execution of a subroutine of the original ROM (Step 902), an extended instruction may be called (Y branch of step 904) to perform execution of the patch routine. Thus it can be seen that while the calling subroutine is being executed, the extended instructions are also executed, and when finished the extended instructions return back to the calling ROM subroutine - step 1018.

As per claims 12,22, and 31, **the ROM instructions in the first non-volatile memory portion define a calling ROM based subroutine** (as discussed directly above); **wherein the extended instructions include integrative instructions completing actions** (such as booting) **of the calling ROM based subroutine** (¶5). Wong teaches in ¶5 that the extended instructions maybe be used to fix bugs or add functional enhancements, which therefore lead to the system completing the action of booting (when extended instructions are called from the BROM - ¶40) or completing a processor function (when extended instructions are called from the PROM -¶40).

As per claim 25, the rejection follows the rejection of claims 1/16 and claim 2 set forth above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (U.S. Patent Application Publication No. 2004/0210720), as applied to claim 1 above, in view of Ewertz et al. (U.S. Patent No. 6,536,038).

As per claim 15, Wong does not specifically teach the first non-volatile memory portion comprising an electrically erasable and rewritable memory (i.e. EEPROM or flash). Ewertz teaches a method for updating firmware (i.e. ROM, flash, EEPROM, etc - column 1, lines 33-39). It would have been obvious to one having ordinary skill in the art at the time the invention

was made to have combined the system of Wong with the EEPROM teaching of Ewertz to have used a flash memory instead of a ROM (BROM/PROM) as the first non-volatile memory portion, as portions of the non-volatile memory could have been rewritten or reused (column 3, line 59 - column 4, line 34), while a portion of the flash could have been locked and unable to be reprogrammed for security purposes or the like (such as the BROM and PROM of Wong).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas
Patent Examiner

16 August 2007